5-mW and 5% Efficiency 216-GHz InP-Based Heterostructure Barrier Varactor Tripler

X. Mélique, C. Mann, P. Mounaix, J. Thornton, O. Vanbésien, F. Mollot, and D. Lippens

***Abstract*—We report on record performance in terms of efficiency and output power for an InP-based heterostructure barrier varactor (HBV) tripler. Owing to a step-like InGaAs/InAlAs/AlAs barrier scheme, the device exhibits excellent voltage handling with low leakage current (10 A/cm^2) up to at least 5 V. A 4×12 μm^2 finger-shaped device in a dual configuration yielded a delivered output power of 5 mW (5.4% conversion efficiency) at 216 GHz.**

***Index Terms*—HBV's, InP-based materials, varactor tripler.**

I. Introduction

WHISKER-CONTACTED [1], [2] or planar-integrated [3], [4] GaAs-based heterostructure barrier varactors (HBV's) have now shown promise for millimeter-wave operation and have key advantages over Schottky barrier varactors in terms of device functionality (only the odd-harmonics are generated) and of epitaxial integration. A major limitation of GaAs-HBV's, however, stems from their relatively high leakage current. This is primarily due to the limited barrier height and to parasitic current contributions which involve Γ-X mixing effects. When these devices are used for harmonic multiplication, the nonup-converted power raises the junction temperature resulting in a higher leakage current through thermal emission leading to a dramatic degradation of performance. InP-based HBV's may alleviate such a drawback primarily because the height of the blocking barrier, which prevents conduction through the structure, is high, while each cladding layer can be depleted according to the bias condition.

There has been a great deal of work in determining an effective means to maintain the leakage current at a low level. The desired goal is to provide a barrier thick enough without sacrificing the benefits of a high barrier discontinuity. The step-like barrier scheme induced by the growth of InGaAs/InAlAs/AlAs heterojunctions allows such a criteria to be met [5], [6]. The frequency tripler, described here, uses such InAlAs/InGaAs heterojunctions with a thin AlAs layer in the middle of the barrier. The associated benefit is a high voltage handling capability before significant conduction which permits us to demonstrate the best planar HBV's results reported to date above 200 GHz.

II. Integration Techniques

The technology demonstrated in this letter starts from the epitaxial material reported in [6]. In short, the blocking barrier consists of an $In_{0.52}Al_{0.48}As$ 5-nm-thick/AlAs 3-nm-thick/$In_{0.52}Al_{0.48}As$ 5-nm-thick trilayered heterostructure. This blocking layer was sandwiched between two 300-nm-thick cladding layers whose doping concentration was typically 1×10^{17} cm^{-3}. This basic scheme was grown two times in sequence so that a dual configuration (two diodes epitaxially stacked) is thus obtained. In addition, a 0.5-μm-thick capping layer and 1-μm-thick buried layer with an n-doping concentration of 5×10^{18} cm^{-3} are grown in order to implement low-resistance contact regions.

The main effort on device fabrication concerns the technological procedures aimed at planar integration of the devices by means of a low-parasitic air-bridge technique. To this aim, we developed a pyrolyzation technique [7] with Hoescht photoresists. Pyrolyzation of photolithography patterned resists results in a convex-shaped temporary mold for evaporated thin metal films. Such a procedure permitted us to fabricate, with a relatively high-yield finger-shaped (4-μm width), or round-shaped devices. In addition, the single devices, which already contain two epitaxially stacked barriers as aforementioned, can be further series integrated by placing two devices facing each other. A scanning electron microphotograph of this configuration is displayed in Fig. 1. Otherwise, conventional fabrication processes including notably electron beam patterning and nonselective reactive ion etching were used to process the 2-in wafer using six mask levels.

III. RF Measurements

The radio frequency (RF) assessment of the devices was carried out in two stages including on-wafer probing techniques [8] and characterization of samples mounted in a multiplier block. For the former, the measurements were performed up to 110 GHz, so that the intrinsic capacitance and the series resistance which are key figures of merit in the frequency capability of the devices can be accurately determined. Fig. 2

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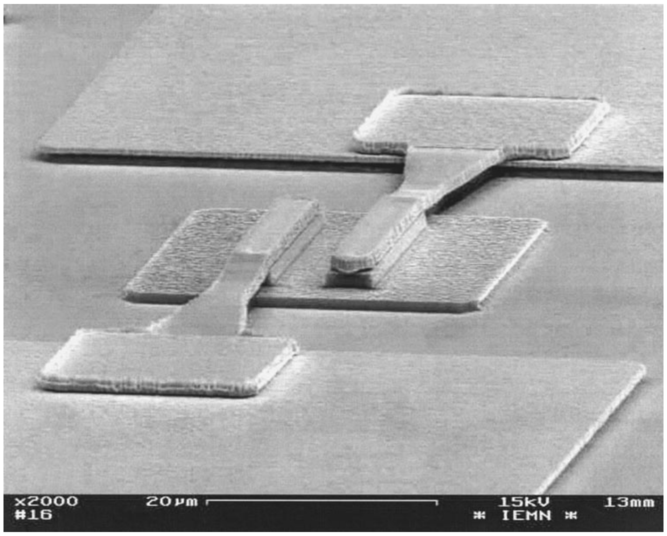

Fig. 1. SEM view of a four-barrier device (two epitaxially stacked and two planar integrated barriers). The finger dimensions are 4×12 μm^2, and the mesa is 1.5 μm high.

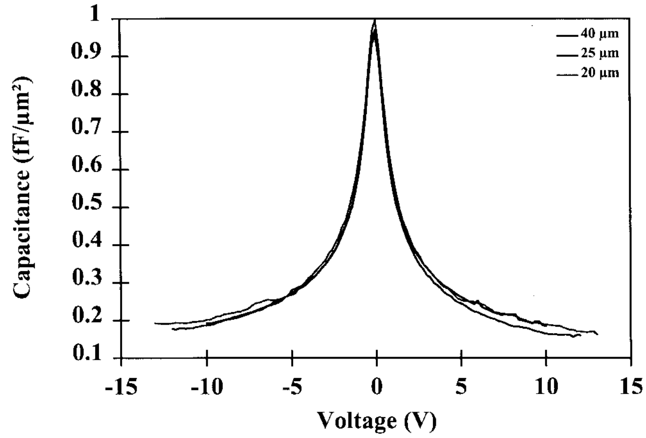

Fig. 2. Typical $C(V)$ characteristic of a single heterostructure barrier varactor (dual barrier) for different diode diameters.

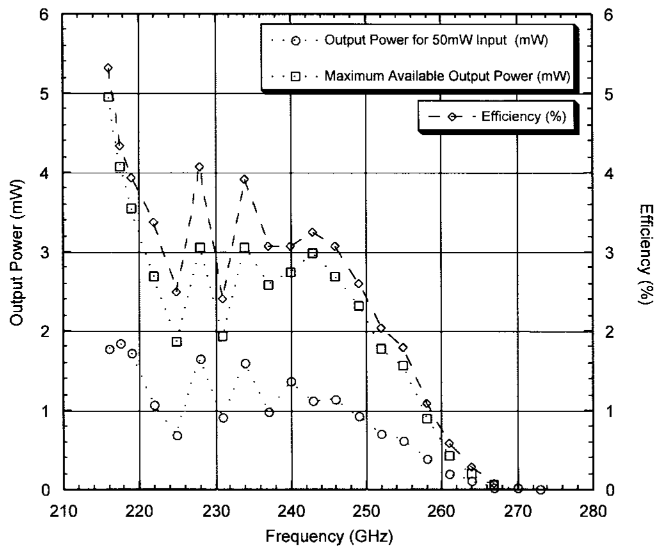

Fig. 3. Output power and conversion efficiency versus output frequency.

illustrates the capacitance voltage characteristics of a typical dual-barrier device. We thus found an intrinsic capacitance level of typically 1 fF/μm^2 for a single sample (two barriers) along with a capacitance ratio of 5 : 1. The breakdown voltage reaches 12 V. Electrical measurements versus temperature demonstrate that impact ionization in the depleted zone is responsible for this breakdown process. The series resistance does not scale with the area and hence was found dominated by the spreading contribution. For a typical 50-μm^2 area device with a distance between the mesa and the side ohmic contact of 5 μm, the best series resistance value was found to be as low as 2.5 Ω. In practice, this key figure of merit was deduced using the deembedding procedure described in [8]. Such a promising result can be explained first by the use of a low gap (Eg $=$ 0.7 eV), highly doped (5×10^{18} cm^{-3}), thick (1 μm), InGaAs buried layer lattice matched to InP. For instance, the ohmic contact resistance which can be deduced from TLM measurements can be as low as 1.5×10^{-7} Ω·cm^2 with Ni/Ge/Au/Ti/Au ohmic contact material annealed at 400°C for 40 s.

For the mounting of the devices into the multiplier block, the samples were first diced with a typical track depth of 5 μm. Then they were lapped to a thickness of 100 μm by HCl wet etching and finally separated into discrete chips by cleaving. The overall chip dimensions are $100 \times 220 \times 100$ μm^3.

The tripler block used was a Rutherford Appleton Laboratory waveguide block described in detail elsewhere [9]. It was equipped with a single backshort at the output and both backshort and E-plane tuners at the input. Input power was delivered by a Carlstrom Gunn Oscillator (serial number H279) which could be mechanically tuned over the frequency range of 72–96 GHz and gives around 100 mW from 72 to 89 GHz. Both input and output powers were measured using separate Anritsu power heads which have been previously compared with a Thomas Keating power meter. To date, a maximum output power 5 mW was obtained at a pump frequency of 72 GHz ($F_{\rm out} = 216$ GHz). However, a maximum output power greater than $\sim$2 mW was generated from 216 to 250 GHz as shown in Fig. 3. Also plotted in this figure is the output power for 50 mW input. Above 250 GHz, we observed a sharp decrease in output power even though the waveguide circuit has previously operated to over 300 GHz using GaAs based HBV's [10]. This discrepancy is attributed to the thicker substrate (100 μm versus 50 μm) which has not been accounted for electrically. We are currently further thinning the samples to test the validity of this assumption.

Fig. 4 shows the variation of the output power and of the overall efficiency measured at 216 GHz versus input power. The efficiency exhibits a steep increase for input power in excess of 20 mW and then saturates when the input powers reaches 100 mW. The maximum conversion efficiency is 5.4%, whereas the delivered power is more or less increasing linearly. In the present experiment which was limited by available input power, a maximum output power of 5 mW is thus obtained in the lower part of the spectrum. To the best of our knowledge, this is the highest performance published so far for heterostructure barrier varactor in this

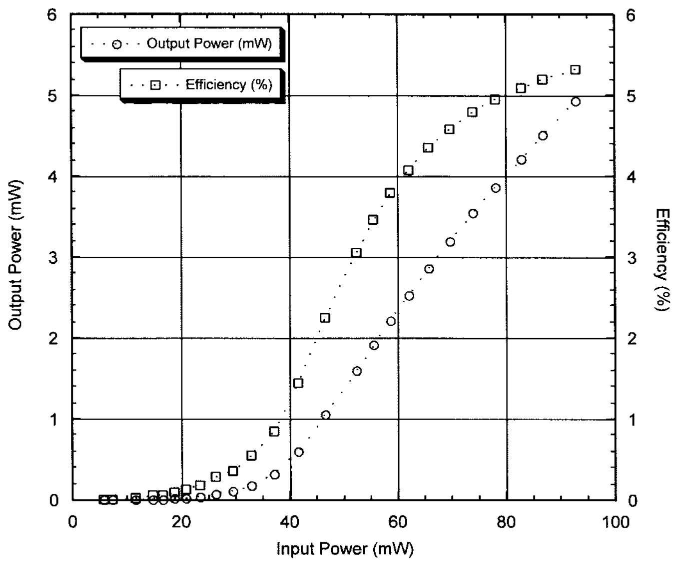

Fig. 4. Conversion efficiency and output power as a function of input power.

frequency range. The voltage, and hence power handling, of the device under test is the main reason for this improvement in performance. Indeed, when the devices exhibit a high leakage current, combined with a large increase in temperature through thermally activated leakage mechanisms, a degradation of conversion efficiency can be expected for increased input powers. The so-called self-heating effects were addressed recently for UVA-NRL 1174 GaAs/$Al_{0.75}Ga_{0.25}As$ HBV's [11]. For the present InAlAs/AlAs/InAlAs devices the activation energy for the resonant tunneling process, which is responsible for the leakage current at a low voltage is of about 600 meV. Further details concerning this issue can be found in [12]. Also, systematic studies of basic device behavior (one single barrier) as a function of temperature show that the leakage current increases by about a decade when the device temperature is increased from 300K (J ~ 0.8 A/cm^2) to 415K (J $\sim$ 7 A/cm^2) at a bias voltage of 3.5 V. Under these conditions, it is believed that the thermal degradation effects will occur at much higher pump powers with the associated benefit of an increase in the delivered power by the diode. In addition, the use of InP-based material is extremely favorable for obtaining a higher cutoff frequency. For the present work, a cutoff frequency of 2 THz can be calculated for single devices assuming $R_s = 2.5\ \Omega$, C_{j0} = 1 fF/μm^2 and a capacitance ratio of 5 : 1. Harmonic balance simulations were carried out by means of the commercial software Microwave Design System from Hewlett Packard, on the basis of this data. They predict a maximum efficiency of about 22% implying an additional conversion loss of ~6 dB. Much of this can be attributed to the waveguide mount, notably, mismatch in the input and output circuits, ohmic and dielectric loss, and finally loss in the backshort tuning mechanism. These elements will now be optimized, the aim being to reduce them to their theoretical limits.

IV. CONCLUSION

High-performance InGaAs/InAlAs heterostructure barrier varactor diodes having a thin AlAs barrier in the middle of the barrier have been fabricated and RF tested. Preliminary tripler measurements carried out for input frequencies between 72 and 83 GHz are very promising. A conversion efficiency in excess of 5% at 216 GHz was obtained giving an output power of 5 mW. It is believed that further improvements in these performances can be achieved via careful optimization of the waveguide circuit. In addition, a linear increase in the output power was demonstrated implying that increased output power levels could have been attained had higher pump levels been available.

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